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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,759	12/03/2003	Carlos Gonzalez	SNDK.234US2	7564

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EXAMINER
PORTKA, GARY J

ART UNIT	PAPER NUMBER
2188	

Gerald P. Parsons
Hsue & de Runtz LLP
Suite 1800
655 Montgomery Street
San Francisco, CA 94111

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,759	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Gary J. Portka	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12//3/03,8/8/05, &.* 9/28/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14 are presented for examination.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on December 3, 2003, August 8, 2005, and September 28, 2005, were considered by the examiner, except that in the latter all foreign patent documents were not considered since no copies, statements of relevance, or translations were provided, and document 8 therein is duplicated from another IDS page.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 7 recite "programmable in units of an integer number of a plurality of pages". The disclosure states that a page may be entirely simultaneously programmed, or programmed in chunks of the page (page 8 lines 6-9); the first embodiment further appears to define a page as the smallest unit programmable in one operation (page 12 lines 3-4). The claim language programmable

unit, however, must be 2 or more pages, which leads to inconsistency and thus indefiniteness of the meaning of the claimed page.

Claims 1 and 7 also recite "sector" and a relationship between it and the programmable and erasable units of the memory. While "sector" for hard disks is well defined in the art, the translation into semiconductor memory is not. The present disclosure defines sector as what user data are typically transferred in between host and memory, and can be any amount convenient to handle (page 1 lines 34-37). Thus, it is not clear what differentiates the claimed sector from any successive data transferred from at least parts of two pages, making the claim language vague and indefinite.

Claims 2-6 and 8-14 incorporate the limitations of claims 1 and 7 and therefore are rejected for the same reasons.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Fukuzumi, U.S. Patent 6,434,658 B1.

8. As to claim 1, Fukuzumi discloses a method of operating a memory having a plurality of cells organized into blocks containing a minimum number of cells simultaneously erasable (see col. 1 lines 19-21) with minimum programmable units of an integer number of pages (the 2048 byte sector of the flash), comprising programming individual sectors of data containing less than the page amount of data across boundaries of the pages, where a block has more sectors than pages. As shown in Figure 2, the flash programmable size of 2048 bytes is the recited page, and the recited sector containing less than the page amount of data may be considered each consecutive group of three 512 byte medium sectors, for example one sector as addresses 0h, 1h, and 2h, the next sector as addresses 3h, 4h, and 5h, etc. (since the term "sector" is broadly defined as any amount of data that is less than the given amount of data in a page). See also the Abstract, Fig. 1, col. 1 lines 29-40, col. 2 lines 28-34, col. 4 lines 64-67, col. 5 lines 4-21, and col. 7 lines 1-42.

9. Claims 7-11 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Sukegawa et al., U.S. Patent 5,603,001.

10. As to claim 7, Sukegawa discloses an operating method for a memory with cells organized into blocks containing smallest group of cells simultaneously erasable, programmable in units of integer number of pages, comprising programming sectors containing more than the page amount of data across boundaries of the pages (see Abstract, Figures 1, 3, and 7, column 1 lines 30-35 and 45-50, column 2 lines 29-41,

column 14 lines 52-63, column 20 lines 20-30 and 37-40, and column 20 line 59 to column 21 line 20).

11. As to claim 8, the claimed sectors in Sukegawa may be considered the entirety of the data shown in the pages in Figure 7, and thus containing all the recited data.

12. As to claims 9-11, Sukegawa discloses the limitations to the extent claimed since each of the pages, and each of the blocks shown in Figure 7 may contain the data recited.

13. As to claim 13, Sukegawa discloses plurality of pages per block as cited above.

14. Claims 7-11 are rejected under 35 U.S.C. 102(a) as being anticipated by Sinclair et al., WO 00/49488.

15. As to claim 7, Sinclair discloses a method of operating a memory having a plurality of cell organized into blocks of a minimum number of cells simultaneously erasable (see Fig. 35, and pages 61 line 20 to page 62 line 19) with minimum programmable units of an integer number of pages, comprising programming individual sectors of data across boundaries of the pages. Sinclair also teaches that the sector size may be larger than than the programmable page size (page 12 lines 1-4), and that the two need not have any relation (page 62).

16. As to claims 8-11, Sinclair teaches user data and attributes/overhead as recited (see Figs. 3, 4, 28-31(b), and 33)

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sinclair et al., WO 00/49488.

19. As to claim 1, Sinclair discloses a method of operating a memory having a plurality of cell organized into blocks of a minimum number of cells simultaneously erasable (see Fig. 35, and pages 61 line 20 to page 62 line 19) with minimum programmable units of an integer number of pages, comprising programming individual sectors of data across boundaries of the pages. Sinclair also teaches that the sector size may be larger than or smaller than the programmable page size (page 12 lines 1-4), and that the two need not have any relation (page 62).

Sinclair does not specifically disclose that the sectors programmed across the page boundaries may be smaller than the page size. However, since Sinclair recognized that sectors slightly larger than the page size are advantageously stored contiguously across pages (Fig. 35), and that sectors might be larger or smaller than the page size (page 12), an artisan would have clearly recognized that sectors of a size smaller than the page size would also advantageously be stored contiguously across the page boundaries (i.e., when the page size is not an integer multiple of the sector size). Such an arrangement maximizes use of storage space and allows complete flexibility in assigning sector sizes, and is enabled by the system of Sinclair to those of ordinary skill in the art. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to store sectors smaller than the page size across page

boundaries, because Sinclair taught storing of sectors across page boundaries, and likewise taught that sectors may be smaller than pages.

20. As to claims 2-5, Sinclair teaches user data and attributes/overhead as recited (see Figs. 3, 4, 28-31(b), and 33)

21. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuzumi, U.S. Patent 6,434,658 B1, in view of Sukegawa et al., U.S. Patent 5,603,001.

22. As to claims 2-5, Fukuzumi teaches the invention substantially as discussed above with regard to claim 1. Fukuzumi does not specifically disclose the limitations of user data and attributes or overhead as recited. However, it was well known to store user data with attributes or overhead in non-volatile flash as recited. For example, the claimed sectors in Sukegawa may be considered the entirety of the data shown in the pages in Figure 7, and thus containing all the recited data; note that Sukegawa discloses the limitations to the extent claimed since each of the pages, and each of the blocks shown in Figure 7 may contain the data recited. The configuration used by Sukegawa for one provides improved defect handling using the shown redundancy area (see column 3 lines 40-45 and column 12 lines 21-27). The improved defect handling would have motivated an artisan to use this configuration in Fukuzumi. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to configure the flash as recited with user data and attribute or overhead areas, because this was previously known to improve defect handling.

23. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuzumi, U.S. Patent 6,434,658 B1, in view of Banks, U.S. Patent 6,356,486 B1.

24. As to claim 6, Fukuzumi does not disclose that the memory cells have more than two threshold levels whereby they each store more than one bit of data. However, it was known in the art that the storage of multiple bits of data per cell increased the capacity or density per cost of memory, and was implemented by Banks in electrically alterable non-volatile memory (to include flash as in Fukuzumi) as taught in Banks Abstract and column 2 lines 39-60. The advantage of increasing the capacity and/or density of the memory in Fukuzumi would have motivated an artisan to implement the memory cells therein to have more than two threshold levels to store more than one bit. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use memory cells having more than two threshold levels storing more than one bit, because this was a known method of increasing the capacity and density of flash memory.

25. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sukegawa et al., U.S. Patent 5,603,001, in view of Miyauchi, U.S. Patent 5,946,714.

26. As to claim 12, Sukegawa does not disclose that blocks include only one page. However, it was well known in the art that the erasable size might contain any desired number of the writable size of a flash memory. As taught by Miyauchi, a prior shortcoming of flash was that write cycles were inefficient because a larger size than the write size was required to be erased before the write, and before the erase occurs data which is not to be changed in the erase block is required to be stored elsewhere

(see column 1 lines 27-36). Miyauchi solves this by making the erase size equal to the write size of a sector (see column 3 lines 21-25, and claim 3); this is equivalent to stating that the erasable block contains only one writable page. An artisan would have been motivated by the improved efficiency of the write cycle to make the block in Sukegawa include only one page. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to have blocks include only one page, because this was a known means of improving efficiency of the write cycle.

27. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sukegawa et al., U.S. Patent 5,603,001, in view of Banks, U.S. Patent 6,356,486 B1.

28. As to claim 14, Sukegawa does not disclose that the memory cells have more than two threshold levels whereby they each store more than one bit of data. However, it was known in the art that the storage of multiple bits of data per cell increased the capacity or density per cost of memory, and was implemented by Banks in electrically alterable non-volatile memory (to include flash as in Sukegawa) as taught in Banks Abstract and column 2 lines 39-60. The advantage of increasing the capacity and/or density of the memory in Sukegawa would have motivated an artisan to implement the memory cells therein to have more than two threshold levels to store more than one bit. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use memory cells having more than two threshold levels storing more than one bit, because this was a known method of increasing the capacity and density of flash memory.

Conclusion

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J. Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary J Portka
Primary Examiner
Art Unit 2188

December 1, 2005

GARY PORTKA
PRIMARY EXAMINER